I. INTRODUCTION

DROP TEST performance has been one of the key package reliability indicators for portable applications. A board-level drop test standard, JESD22-B111, has been published by the Joint Electronic Device Engineering Council (JEDEC) for the components used in handheld electronic products [1]. This allows the evaluation of component (or package) performance under a fixed board and testing condition. There have been numerous studies at component level on the effects of structure, material, and geometry of components [2]–[10]. Component performance at board and system levels, however, becomes even more complicated, since there are many additional factors: the size and thickness of printed circuit board (PCB), major component locations, the placement of

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by changing the distance between the corner components and mounting support locations. Then the effect of secondary components attachment is investigated. Three scenarios to consider the effects of both relative position and size of the secondary components are simulated. Finally, the effects of

in Fig. 4(a). In real-life drops, system board may experience different impact orientations. In this paper, components face-up in a horizontal drop (180° rotation) [Fig. 4(b)], and a vertical drop (90° rotation) [Fig. 4(c)], are studied.

III. Finite Element Models

The details of finite element analysis are referred to the previous papers [7]–[10], [16], [17], [23]. Global and local finite element modeling techniques are applied in this paper. In the global finite element model, the symmetry conditions are applied whenever it is possible to reduce the problem size. A local finite element model is developed at any desired location of the components on the board. Under impact loading, the corner solder balls in a component are usually most vulnerable to crack. Therefore, those solder ball(s) in the local model are created with all necessary information and the refined meshes. Since the primary failure is at the intermetallic layer of solder balls [2], a fixed thickness layer of elements is used at the critical solder ball upper interface to capture the stresses at interface throughout all simulations. Linear elastic implicit dynamic analysis is applied in this paper.

IV. Results

A. Effects of Major Component Locations

Fig. 5 shows the global finite element models of the quarter board assembly, with varying distances $D1$ of 3–9 mm (from the edge of corner component to the mounting hole with respect to x- and y-directions), respectively. As $D1$ increases, the components on the board move away from screw mount and are "squeezed" toward the center of board.

Fig. 6 shows the local finite element model with refined meshes for a corner ball: the outer most corner on the right side, which is expected to be most critical. The local model can be at any locations, for example, at U1 or U8 positions.

Fig. 7(a) plots the peeling stress history of the critical solder ball in the corner component U1 for 12 × 12 array packages (0.5-mm pitch, 6 mm × 6 mm package size). It clearly shows that the distance $D1$ has a significant impact on the solder ball stress, which monotonically decreases with the increase of $D1$. The closer the component U1 is placed to the screw hole, the higher the stress is. Fig. 7(b) shows the peeling stress history of the critical solder ball in the center component U8. Four curves almost coincide with each other. This implies that the ball stress in U8 stays almost the same regardless of $D1$. This is probably due to two reasons: 1) the distance from U8 to mounting hole does not change when $D1$ varies and 2) component U8 is so far away from the mounting hole that the mounting constraint has a negligible effect on the center component.

Fig. 8 plots the maximum peeling stresses with different $D1$ for a package size of 3 mm × 3 mm, 6 mm × 6 mm, and 10 mm × 10 mm, respectively. For these three WLP sizes, the maximum peeling stress at U1 is very sensitive to the distance $D1$, and the stress decreases exponentially with the increased distance. As expected, the maximum peeling stress in U8 stays approximately the same regardless of $D1$ for each package size. From those figures, it is observed that

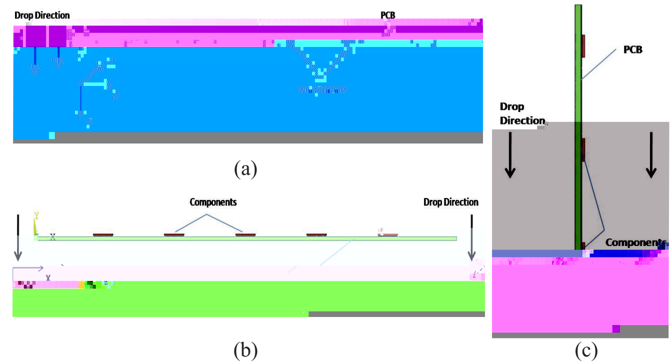


Fig. 4. Drop orientations. (a) Horizontal drop with components face-

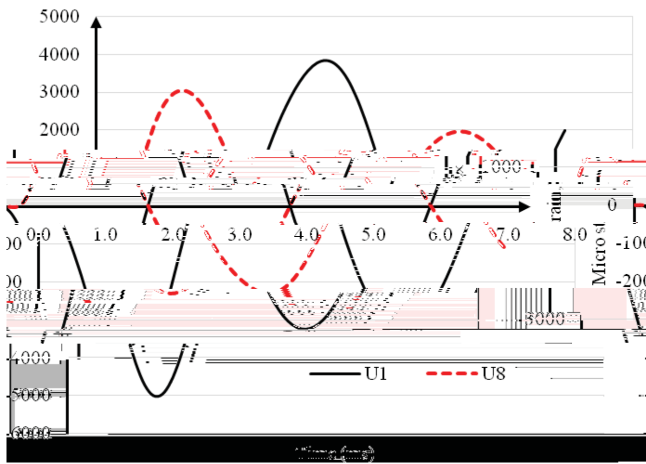
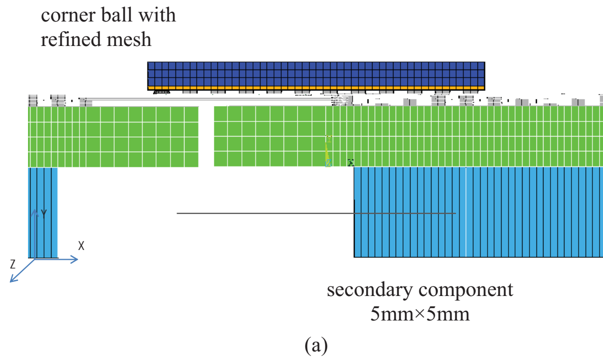


Fig. 9. Board strain component in x-direction in U1 and U8 (12×12 array package, $D1 = 5$ mm).



(a)

(b)

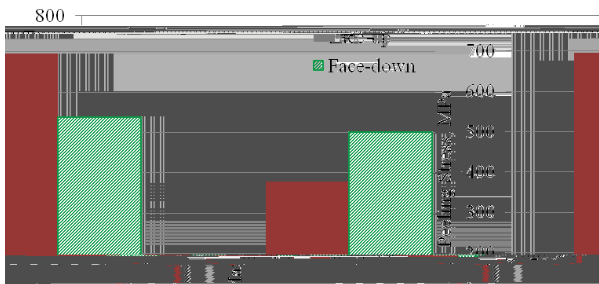


Fig. 18. Maximum tensile stresses in U1 and U8 on JEDEC drop test board.

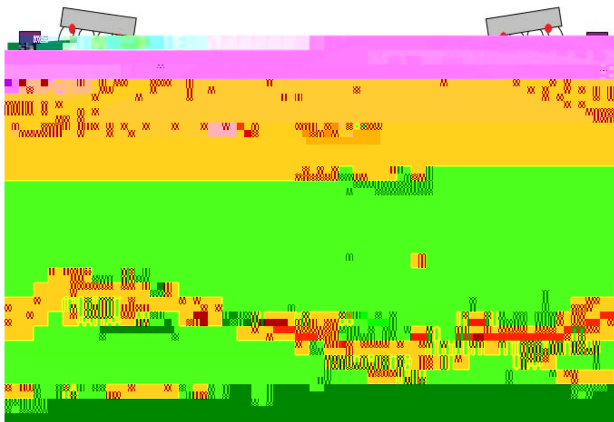


Fig. 19. Illustration of solder ball damages for component face-down and face-up configurations.

Solder balls experience tensile stress when the board